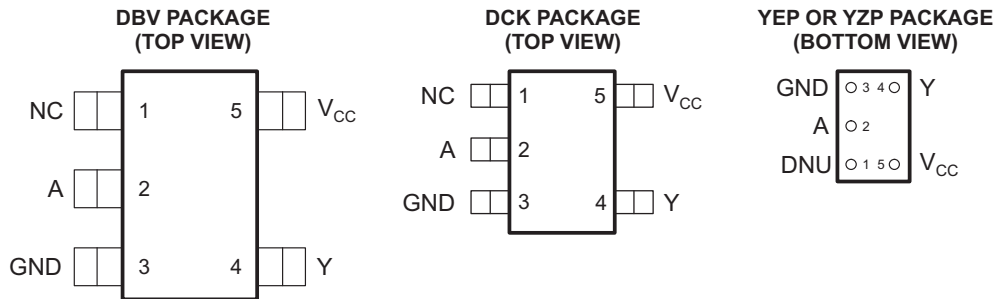


**FEATURES**

- Available in the Texas Instruments NanoStar™ and NanoFree™ Packages
- Low Static-Power Consumption ( $I_{CC} = 0.9 \mu\text{A Max}$ )
- Low Dynamic-Power Consumption ( $C_{pd} = 1 \text{ pF Typ at } 3.3 \text{ V}$ )
- Low Input Capacitance ( $C_i = 1.5 \text{ pF Typ}$ )
- Low Noise – Overshoot and Undershoot <10% of  $V_{CC}$
- $I_{off}$  Supports Partial Power-Down-Mode Operation
- Input Hysteresis Allows Slow Input Transition and Better Switching Noise Immunity at the Input ( $V_{hys} = 250 \text{ mV Typ at } 3.3 \text{ V}$ )
- Wide Operating  $V_{CC}$  Range of 0.8 V to 3.6 V
- Optimized for 3.3-V Operation
- 3.6-V I/O Tolerant to Support Mixed-Mode Signal Operation
- $t_{pd} = 3.6 \text{ ns Max at } 3.3 \text{ V}$
- Suitable for Point-to-Point Applications
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Performance Tested Per JESD 22
  - 2000-V Human-Body Model (A114-B, Class II)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)
- ESD Protection Exceeds  $\pm 5000 \text{ V}$  With Human-Body Model



See mechanical drawings for dimensions.  
NC – No internal connection  
DNU – Do not use

**DESCRIPTION/ORDERING INFORMATION**

The AUP family is TI's premier solution to the industry's low-power needs in battery-powered portable applications. This family ensures a very low static and dynamic power consumption across the entire  $V_{CC}$  range of 0.8 V to 3.6 V, resulting in an increased battery life. This product also maintains excellent signal integrity (see Figure 1 and Figure 2).

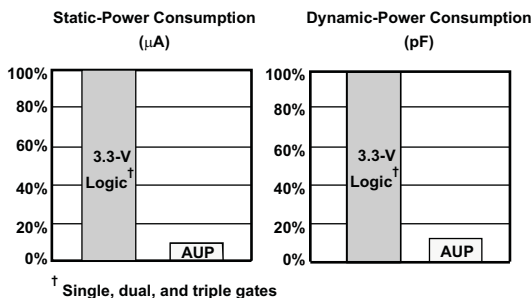


Figure 1. AUP – The Lowest-Power Family

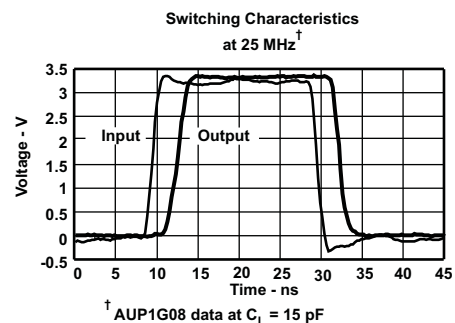


Figure 2. Excellent Signal Integrity



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

NanoStar, NanoFree are trademarks of Texas Instruments.

# SN74AUP1G06

## LOW-POWER SINGLE INVERTER BUFFER/DRIVER WITH OPEN-DRAIN OUTPUTS

SCES590A–JULY 2004–REVISED AUGUST 2006

### DESCRIPTION/ORDERING INFORMATION (CONTINUED)

The output of this single inverter buffer/driver is open drain, and can be connected to other open-drain outputs to implement active-low wired-OR or active-high wired-AND functions.

NanoStar™ and NanoFree™ package technology is a major breakthrough in IC packaging concepts, using the die as the package.

This device is fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

### ORDERING INFORMATION

$T_A$	PACKAGE <sup>(1)</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING <sup>(2)</sup>
–40°C to 85°C	NanoStar™ – WCSP (DSBGA) 0.23-mm Large Bump – YEP	Reel of 3000	SN74AUP1G06YEPR <sup>(3)</sup>	_ _ _ HT _
	NanoFree™ – WCSP (DSBGA) 0.23-mm Large Bump – YZP (Pb-free)		SN74AUP1G06YZPR <sup>(3)</sup>	
	SOT (SOT-23) – DBV	Reel of 3000	SN74AUP1G06DBVR	H06_
		Reel of 250	SN74AUP1G06DBVT	
	SOT (SC-70) – DCK	Reel of 3000	SN74AUP1G06DCKR	HT_
		Reel of 250	SN74AUP1G06DCKT	

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).

(2) DBV/DCK: The actual top-side marking has one additional character that designates the assembly/test site.

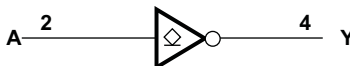
YEP/YZP: The actual top-side marking has three preceding characters to denote year, month, and sequence code, and one following character to designate the assembly/test site. Pin 1 identifier indicates solder-bump composition (1 = SnPb, • = Pb-free).

(3) Package preview

### FUNCTION TABLE

INPUT A	OUTPUT Y
H	L
L	H

### LOGIC DIAGRAM (POSITIVE LOGIC)



**Absolute Maximum Ratings<sup>(1)</sup>**

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage range	–0.5	4.6	V
$V_I$	Input voltage range <sup>(2)</sup>	–0.5	4.6	V
$V_O$	Voltage range applied to any output in the high-impedance or power-off state <sup>(2)</sup>	–0.5	4.6	V
$V_O$	Output voltage range in the high or low state <sup>(2)</sup>	–0.5	$V_{CC} + 0.5$	V
$I_{IK}$	Input clamp current	$V_I < 0$	–50	mA
$I_{OK}$	Output clamp current	$V_O < 0$	–50	mA
$I_O$	Continuous output current		±20	mA
	Continuous current through $V_{CC}$ or GND		±50	mA
$\theta_{JA}$	Package thermal impedance <sup>(3)</sup>	DBV package	206	°C/W
		DCK package	252	
		YEP/YZP package	132	
$T_{stg}$	Storage temperature range	–65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The package thermal impedance is calculated in accordance with JESD 51-7.

**Recommended Operating Conditions<sup>(1)</sup>**

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage	0.8	3.6	V
$V_{IH}$	High-level input voltage	$V_{CC} = 0.8$ V	$V_{CC}$	V
		$V_{CC} = 1.1$ V to 1.95 V	$0.65 \times V_{CC}$	
		$V_{CC} = 2.3$ V to 2.7 V	1.6	
		$V_{CC} = 3$ V to 3.6 V	2	
$V_{IL}$	Low-level input voltage	$V_{CC} = 0.8$ V	0	V
		$V_{CC} = 1.1$ V to 1.95 V	$0.35 \times V_{CC}$	
		$V_{CC} = 2.3$ V to 2.7 V	0.7	
		$V_{CC} = 3$ V to 3.6 V	0.9	
$V_I$	Input voltage	0	3.6	V
$V_O$	Output voltage	0	3.6	V
$I_{OL}^{(2)}$	Low-level output current	$V_{CC} = 0.8$ V	20	mA
		$V_{CC} = 1.1$ V	1.1	
		$V_{CC} = 1.4$ V	1.7	
		$V_{CC} = 1.65$ V	1.9	
		$V_{CC} = 2.3$ V	3.1	
		$V_{CC} = 3$ V	4	
$\Delta t/\Delta v$	Input transition rise or fall rate	$V_{CC} = 0.8$ V to 3.6 V	200	ns/V
$T_A$	Operating free-air temperature	–40	85	°C

- (1) All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.
- (2) Defined by the signal integrity requirements and design-goal priorities

# SN74AUP1G06

## LOW-POWER SINGLE INVERTER BUFFER/DRIVER WITH OPEN-DRAIN OUTPUTS

SCES590A–JULY 2004–REVISED AUGUST 2006

### Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C			T <sub>A</sub> = -40°C to 85°C		UNIT
			MIN	TYP	MAX	MIN	MAX	
V <sub>OL</sub>	I <sub>OL</sub> = 20 μA	0.8 V to 3.6 V			0.1		0.1	V
	I <sub>OL</sub> = 1.1 mA	1.1 V			0.3 × V <sub>CC</sub>		0.3 × V <sub>CC</sub>	
	I <sub>OL</sub> = 1.7 mA	1.4 V			0.31		0.37	
	I <sub>OL</sub> = 1.9 mA	1.65 V			0.31		0.35	
	I <sub>OL</sub> = 2.3 mA	2.3 V			0.31		0.33	
	I <sub>OL</sub> = 3.1 mA				0.44		0.45	
	I <sub>OL</sub> = 2.7 mA	3 V			0.31		0.33	
	I <sub>OL</sub> = 4 mA				0.44		0.45	
I <sub>I</sub>	A input	V <sub>I</sub> = GND to 3.6 V			0.1		0.5	μA
I <sub>off</sub>		V <sub>I</sub> or V <sub>O</sub> = 0 V to 3.6 V			0.2		0.6	μA
ΔI <sub>off</sub>		V <sub>I</sub> or V <sub>O</sub> = 0 V to 3.6 V			0.2		0.6	μA
I <sub>CC</sub>		V <sub>I</sub> = GND or V <sub>CC</sub> to 3.6 V, I <sub>O</sub> = 0			0.5		0.9	μA
ΔI <sub>CC</sub>		V <sub>I</sub> = V <sub>CC</sub> - 0.6 V, I <sub>O</sub> = 0			40		50	μA
C <sub>i</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	0 V		1.5				pF
		3.6 V		1.7				
C <sub>o</sub>	V <sub>O</sub> = GND	0 V		1.7				pF

### Switching Characteristics

over recommended operating free-air temperature range, C<sub>L</sub> = 5 pF (unless otherwise noted) (see Figure 3 and Figure 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub>	T <sub>A</sub> = 25°C			T <sub>A</sub> = -40°C to 85°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
t <sub>pd</sub>	A	Y	0.8 V		12.4				ns
			1.2 V ± 0.1 V	2.7	12	9.9	2	12.8	
			1.5 V ± 0.1 V	2.1	3.5	6.2	1.5	7.6	
			1.8 V ± 0.15 V	2.1	3.1	4.7	1.2	5.9	
			2.5 V ± 0.2 V	1.4	2.2	3.2	1	3.9	
			3.3 V ± 0.3 V	1.3	2.2	3.3	0.8	3.6	

### Switching Characteristics

over recommended operating free-air temperature range, C<sub>L</sub> = 10 pF (unless otherwise noted) (see Figure 3 and Figure 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub>	T <sub>A</sub> = 25°C			T <sub>A</sub> = -40°C to 85°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
t <sub>pd</sub>	A	Y	0.8 V		15.1				ns
			1.2 V ± 0.1 V	3.6	12	11.2	2.7	14.1	
			1.5 V ± 0.1 V	2.9	4.3	7	2.2	8.6	
			1.8 V ± 0.15 V	2.7	3.9	5.4	1.8	6.7	
			2.5 V ± 0.2 V	2.1	2.9	3.8	1.4	4.5	
			3.3 V ± 0.3 V	1.7	3	4.5	1.2	4.9	

### Switching Characteristics

over recommended operating free-air temperature range,  $C_L = 15$  pF (unless otherwise noted) (see [Figure 3](#) and [Figure 4](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC}$	$T_A = 25^\circ\text{C}$			$T_A = -40^\circ\text{C}$ to $85^\circ\text{C}$		UNIT
				MIN	TYP	MAX	MIN	MAX	
$t_{pd}$	A	Y	0.8 V	17.4					ns
			$1.2\text{ V} \pm 0.1\text{ V}$	4.9	12	12.2	3.4	15.2	
			$1.5\text{ V} \pm 0.1\text{ V}$	3.5	5	7.7	2.7	9.4	
			$1.8\text{ V} \pm 0.15\text{ V}$	3.2	4.8	6.6	2.2	7.3	
			$2.5\text{ V} \pm 0.2\text{ V}$	2.5	3.5	4.5	1.7	5.1	
			$3.3\text{ V} \pm 0.3\text{ V}$	2	3.8	6	1.5	6.5	

### Switching Characteristics

over recommended operating free-air temperature range,  $C_L = 30$  pF (unless otherwise noted) (see [Figure 3](#) and [Figure 4](#))

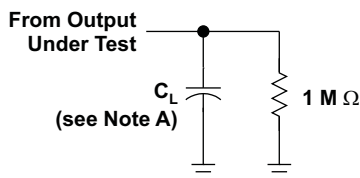
PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC}$	$T_A = 25^\circ\text{C}$			$T_A = -40^\circ\text{C}$ to $85^\circ\text{C}$		UNIT
				MIN	TYP	MAX	MIN	MAX	
$t_{pd}$	A	Y	0.8 V	25.3					ns
			$1.2\text{ V} \pm 0.1\text{ V}$	7.6	12	16	5.6	19.3	
			$1.5\text{ V} \pm 0.1\text{ V}$	5.9	7.6	10.1	4.3	12	
			$1.8\text{ V} \pm 0.15\text{ V}$	4.8	7.4	10.7	3.6	11	
			$2.5\text{ V} \pm 0.2\text{ V}$	3.7	5.4	7.1	2.8	7.8	
			$3.3\text{ V} \pm 0.3\text{ V}$	3.2	6.5	10.5	2.5	10.8	

### Operating Characteristics

$T_A = 25^\circ\text{C}$

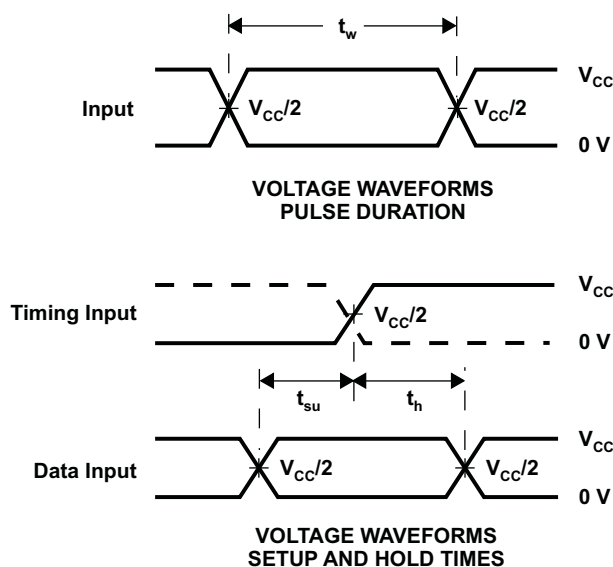
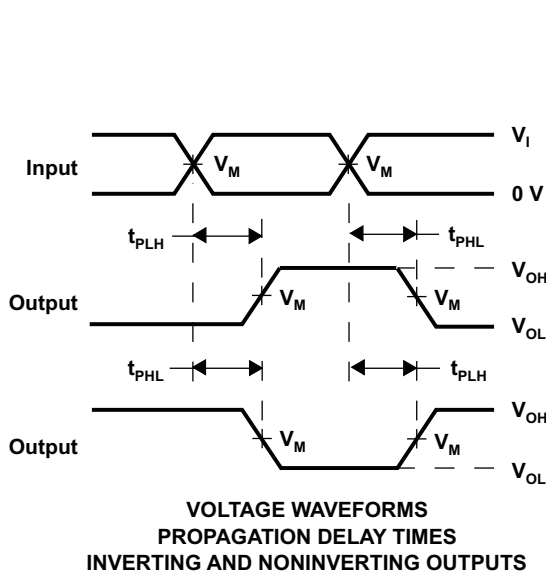
PARAMETER		TEST CONDITIONS	$V_{CC}$	TYP	UNIT
$C_{pd}$	Power dissipation capacitance	$f = 10\text{ MHz}$	0.8 V	1	pF
			$1.2\text{ V} \pm 0.1\text{ V}$	1	
			$1.5\text{ V} \pm 0.1\text{ V}$	1	
			$1.8\text{ V} \pm 0.15\text{ V}$	1	
			$2.5\text{ V} \pm 0.2\text{ V}$	1	
			$3.3\text{ V} \pm 0.3\text{ V}$	1	

**PARAMETER MEASUREMENT INFORMATION**  
**(Propagation Delays, Setup and Hold Times, and Pulse Width)**



**LOAD CIRCUIT**

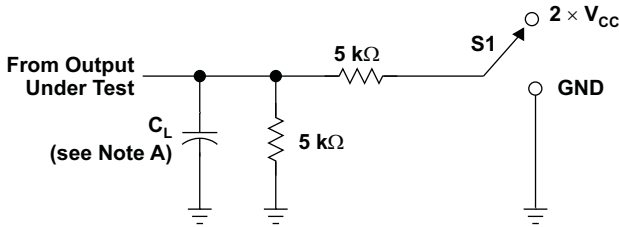
	$V_{CC} = 0.8 \text{ V}$	$V_{CC} = 1.2 \text{ V}$ $\pm 0.1 \text{ V}$	$V_{CC} = 1.5 \text{ V}$ $\pm 0.1 \text{ V}$	$V_{CC} = 1.8 \text{ V}$ $\pm 0.15 \text{ V}$	$V_{CC} = 2.5 \text{ V}$ $\pm 0.2 \text{ V}$	$V_{CC} = 3.3 \text{ V}$ $\pm 0.3 \text{ V}$
$C_L$	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF
$V_M$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$
$V_I$	$V_{CC}$	$V_{CC}$	$V_{CC}$	$V_{CC}$	$V_{CC}$	$V_{CC}$



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
B. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r/t_f = 3 \text{ ns}$ .  
C. The outputs are measured one at a time, with one transition per measurement.  
D.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .  
E. All parameters and waveforms are not applicable to all devices.

**Figure 3. Load Circuit and Voltage Waveforms**

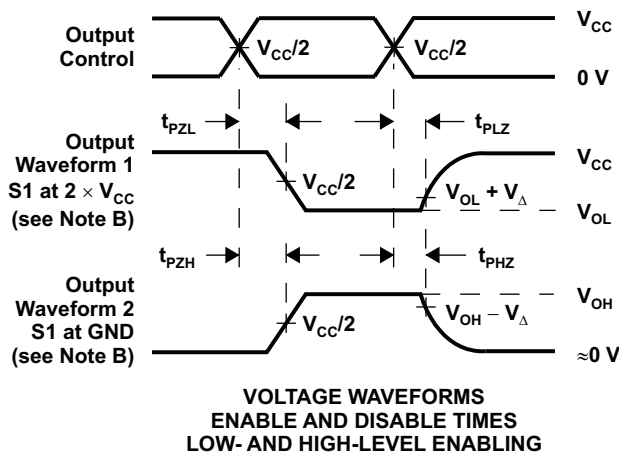
PARAMETER MEASUREMENT INFORMATION  
(Enable and Disable Times)



TEST	S1
$t_{PLZ}/t_{PZL}$	$2 \times V_{CC}$
$t_{PHZ}/t_{PZH}$	GND

LOAD CIRCUIT

	$V_{CC} = 0.8 \text{ V}$	$V_{CC} = 1.2 \text{ V}$ $\pm 0.1 \text{ V}$	$V_{CC} = 1.5 \text{ V}$ $\pm 0.1 \text{ V}$	$V_{CC} = 1.8 \text{ V}$ $\pm 0.15 \text{ V}$	$V_{CC} = 2.5 \text{ V}$ $\pm 0.2 \text{ V}$	$V_{CC} = 3.3 \text{ V}$ $\pm 0.3 \text{ V}$
$C_L$	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF
$V_M$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$
$V_I$	$V_{CC}$	$V_{CC}$	$V_{CC}$	$V_{CC}$	$V_{CC}$	$V_{CC}$
$V_{\Delta}$	0.1 V	0.1 V	0.1 V	0.15 V	0.15 V	0.3 V



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES  
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq 10$  MHz,  $Z_O = 50 \Omega$ ,  $t_r/t_f = 3$  ns.  
 D. The outputs are measured one at a time, with one transition per measurement.  
 E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .  
 F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .  
 G. All parameters and waveforms are not applicable to all devices.

Figure 4. Load Circuit and Voltage Waveforms

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
SN74AUP1G06DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AUP1G06DBVRE4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AUP1G06DBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AUP1G06DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AUP1G06DBVTE4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AUP1G06DBVTG4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AUP1G06DCKR	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AUP1G06DCKRE4	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AUP1G06DCKRG4	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AUP1G06DCKT	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AUP1G06DCKTE4	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AUP1G06DCKTG4	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AUP1G06DRLR	ACTIVE	SOT	DRL	5	4000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AUP1G06DRLRG4	ACTIVE	SOT	DRL	5	4000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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**TAPE AND REEL INFORMATION**



**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AUP1G06DBVR	SOT-23	DBV	5	3000	180.0	9.2	3.23	3.17	1.37	4.0	8.0	Q3
SN74AUP1G06DBVT	SOT-23	DBV	5	250	180.0	9.2	3.23	3.17	1.37	4.0	8.0	Q3
SN74AUP1G06DCKR	SC70	DCK	5	3000	180.0	9.2	2.24	2.34	1.22	4.0	8.0	Q3
SN74AUP1G06DCKT	SC70	DCK	5	250	180.0	9.2	2.24	2.34	1.22	4.0	8.0	Q3
SN74AUP1G06DRLR	SOT	DRL	5	4000	180.0	9.2	1.78	1.78	0.69	4.0	8.0	Q3

**TAPE AND REEL BOX DIMENSIONS**



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AUP1G06DBVR	SOT-23	DBV	5	3000	202.0	201.0	28.0
SN74AUP1G06DBVT	SOT-23	DBV	5	250	202.0	201.0	28.0
SN74AUP1G06DCKR	SC70	DCK	5	3000	202.0	201.0	28.0
SN74AUP1G06DCKT	SC70	DCK	5	250	202.0	201.0	28.0
SN74AUP1G06DRLR	SOT	DRL	5	4000	202.0	201.0	28.0

DBV (R-PDSO-G5)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
  - D. Falls within JEDEC MO-178 Variation AA.

DCK (R-PDSO-G5)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
  - D. Falls within JEDEC MO-203 variation AA.



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- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash, interlead flash, protrusions, or gate burrs. Mold flash, interlead flash, protrusions, or gate burrs shall not exceed 0,15 per end or side.
  - D. JEDEC package registration is pending.

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